MT9512

Programmable Hall Effect Linear Current Sensor IC with Reference Output and High Bandwidth (250kHz)

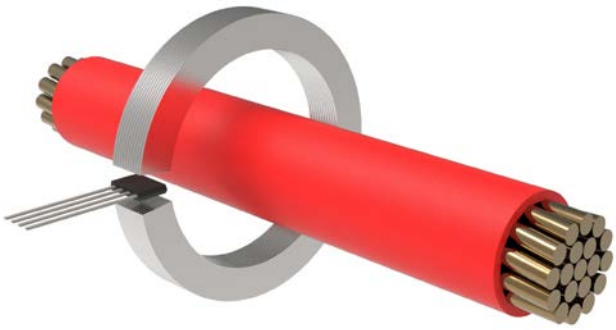
MagnTek | Now Part of NOVOSENSE

1 Product Description

The MagnTek® MT9512 product series is a monolithic programmable Hall effect linear sensor IC. The device can be used for accurate position sensing in a wide range of applications.

Each of the MT9512 consists of a highly sensitive Hall element, a low noise small-signal high-gain amplifier, a clamp and overcurrent protection output stage, and a high bandwidth dynamic offset cancellation technique.

The MT9512 provides an analog output voltage proportional to the applied magnetic flux density. Customers can configure the sensitivity and quiescent (zero field) output voltage through programming on the output pins, to optimize performance in the end application, and the output sensitivity is adjustable within the range of 0.6 to 22.4mV/G. A high-precision interest-bearing reference power supply is integrated into the chip, and its quiescent output voltage and sensitivity do not change with the supply voltage(VCC) . The chip also has its own reference output, allowing the user to easily interact with the ADC or differential op amp using the differential output.



2 Features

- End-of-line programmable
- Typical Accuracy:
  --- ±1.0% (25℃)
- High Linearity:
  --- ±0.2% (25℃)
- High Bandwidth:
  --- 250kHz
- Wide Operating Temperature:
  --- -40℃~150℃
- Fast Output Response Time:
  --- 2.2 μs (typ.)
- Package Option:
  ---SIP-4
- High stability over operation temperature range:
  ---±2.0% (25℃~150℃)
  ---±2.5% (-40℃~25℃)
- Power-independent fixed output mode
- Low-Noise Analog Signal Path
- Reference Output Pin
- RoHS Compliant: (EU)2015/863

3 Applications

- Inverter current sensing
- Motor phase and rail current sensing
- PV string inverters
- Battery management system
- Switching power supplies
- Overcurrent protection

4 Product Overview of MT9512A

Part Number	Sensitivity Range	Package	Packing
MT9512A-01	0.6~1.4 mV/Gs	SIP-4	Bulk packaging(500pcs/bag)
MT9512A-02	1.4~2.8 mV/Gs	SIP-4	Bulk packaging(500pcs/bag)
MT9512A-04	2.8~5.6 mV/Gs	SIP-4	Bulk packaging(500pcs/bag)
MT9512A-08	5.6~11.2 mV/Gs	SIP-4	Bulk packaging(500pcs/bag)
MT9512A-16	11.2~22.4 mV/Gs	SIP-4	Bulk packaging(500pcs/bag)

Table of Contents

Reversion History

1	Originally Version	
2	1.1 Version	Update the definition of TPO; add POR parameters
3	1.2 Version	Corrected the marking error of package information
4	1.3 Version	Update Bulk packaging
5	1.4 Version	Corrected the ESD grade

5 Functional Block Diagram

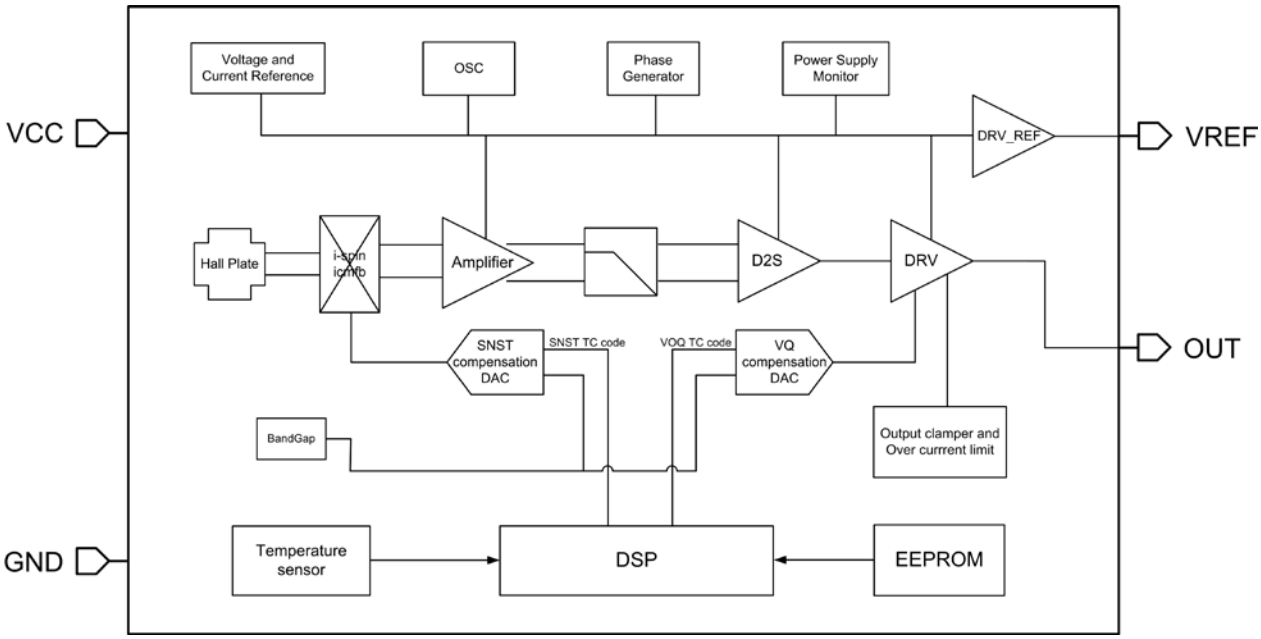
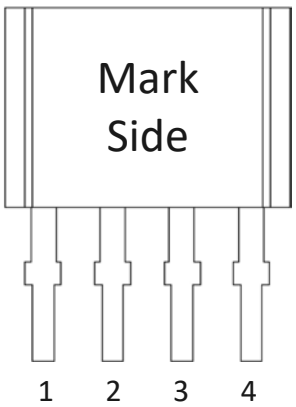


Figure.1 Functional Block Diagram

6 Pin Configuration and Functions



Top View

Figure.2. Pin Configuration & Functions

No.	Name	Description
1	VCC	Power Supply
2	GND	Signal Ground
3	VOUT	Analog Output Signal
4	VREF	Reference Output

7 Transfer Charateristics

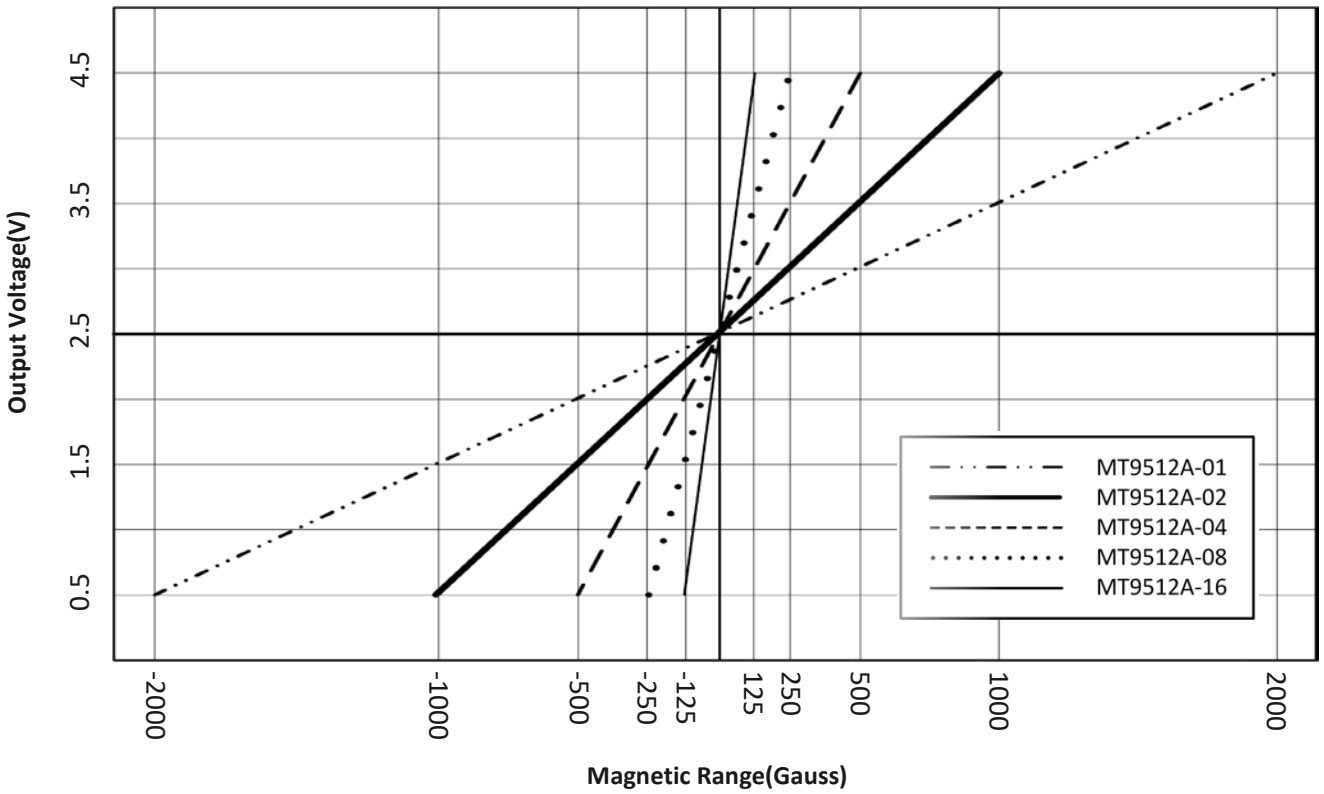


Figure.3 Transfer Characteristics

8 Typical Application Circuit

The typical application circuits of MT9512series products include a bypass capacitor and a filter capacitor as an additional external components. **CBYPASS capacitor between VCC and GND is necessary.**
Magnetic field applied vertically to chip surface, the analog signal output is measured directly from the VOUT pin, and it can also be measured by the difference between VOUT and VREF.

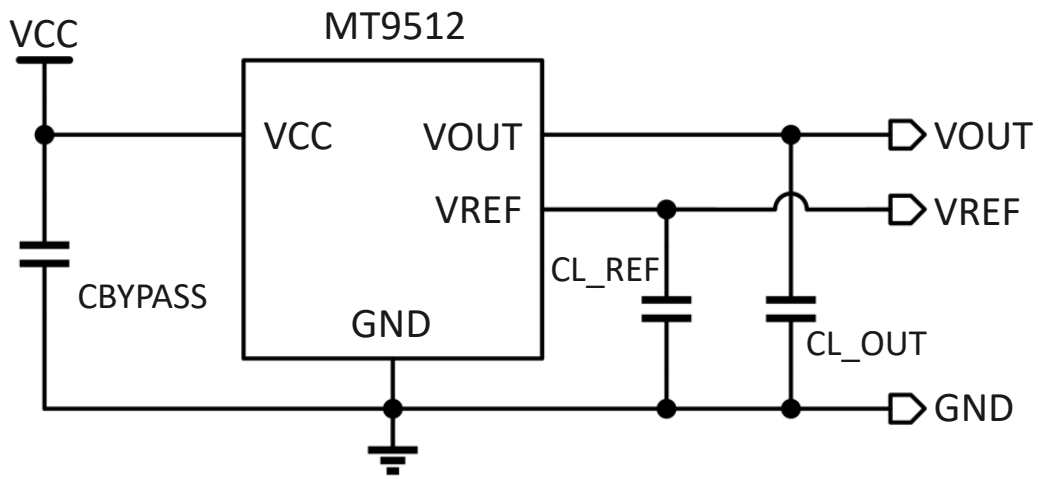


Figure.4 Typical Application Circuit

9 Electrical Magnetic Characteristics

9.1 Absolute Maximum Ratings

Absolute maximum ratings are limited values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

Symbol	Parameters	Min	Max	Units
VCC	Supply Voltage	-	6	V
VRCC	Reverse Battery Voltage	-0.1	-	V
VOUT	Output Voltage	-	VCC+0.5	V
VROUT	Reverse Output Voltage	-0.1	-	V
IOUT(source)	Continuous Output Current(source)	-	55	mA
IOUT(sink)	Continuous Output Current(sink)	-	55	mA
TA	Operating Ambient Temperature	-40	150	℃
TS	Storage Temperature	-50	150	℃
TJ	Junction Temperature	-	165	℃
Endurance	Number of EEPROM Programming Cycles	200	-	cycle

9.2 ESD Ratings

Symbol	Parameters	Reference	Values
VESD	Human-body model(HBM)	AEC-Q100-002	Class 3B
	Charged-device model(CDM)	AEC-Q100-011	Class C3
	Latch up（Latch up）	AEC-Q100-004	Class IIA

9.3 Electrical Specifications

T_A=-40~150 ℃, V_{CC}=5V, C_{BYPASS}=0.1uF (unless otherwise specified)

Symbol	Parameters	Test Condition	Min	Typ	Max	Unit
VCC	Supply Voltage	-	4.5	5	5.5	V
ICC	Supply Current	TA = 25°C	-	12	18	mA
BW	Internal Bandwidth	–3 dB; CL = 1nF	-	250	-	KHz
TPO	Power on time	TA = 25°C, no CBYPASS, CL = 1nF	-	1.3	-	ms
VUVLOH	Undervoltage Lockout(UVLO) High Voltage	TA = 25°C, VCC rising and device function enabled	-	4	-	V
VUVLOL	Undervoltage Lockout(UVLO) Low Voltage	TA = 25°C, VCC falling and device function disabled	-	3.75	-	V
VUVLOHYS	UVLO Hysteresis	TA = 25°C	-	0.25	-	V
TUVLOD	UVLO Delay Time	TA = 25°C	-	30	-	us
VPORH	Power-On Reset High Voltage	TA = 25°C, VCC rising	-	2.75	-	V
VPORL	Power-On Reset Low Voltage	TA = 25°C, VCC falling	-	2.55	-	V
VPORHYS	Power-On Reset Hysteresis	TA = 25°C	-	0.2	-	V
ISCLP	Source Current of Over-Current-Limit	-	-	55	-	mA
ISCLN	Sink Current of Over-Current-Limit	-	-	55	-	mA
TSCLD	Detect Time for over-Current-Limit	TA = 25°C, IOUT>ISCLP or IOUT<ISCLN	-	10	-	us
TSCLR	Release Time for over-Current-Limit	TA = 25°C	-	1	-	ms
VOL	Analog Output Low Saturation Level	RL>=4.7KΩ	-	-	0.3	V
VOH	Analog Output High Saturation Level	RL>=4.7KΩ	VCC-0.3	-	-	V
CL	Output Cap Load	OUT – GND	-	0.47	1	nF
RL	Output Res Load	Pull-down to GND	4.7	-	-	KΩ
		Pull-up to VCC	4.7	-	-	KΩ
ROUT	DC Output resistance	TA=25°C	-	10	-	Ω
CL_REF	Reference Cap Load	VREF–GND	-	0.47	1	nF
RL_REF	Reference Res Load	Pull-down to GND	4.7	-	-	KΩ
		Pull-up to VCC	4.7	-	-	KΩ
ROUT_REF	DC Reference resistance	TA=25°C	-	5	-	Ω
TR	Rise time	B = B(max), TA = 25°C, CL = 1nF	-	1.8	-	us
TPD	Propagation Delay	B = B(max), TA = 25°C, CL = 1nF	-	1.4	-	us
TRESP	Response Time	B = B(max), TA = 25°C, CL = 1nF	-	2.2	-	us

Continued on the next page...

Electrical Specifications(continued)

T_A=-40~150 ℃, V_{CC}=5V, C_{BYPASS}=0.1uF (unless otherwise specified)

Symbol	Parameters	Test Condition	Min	Typ	Max	Unit
VCLP_LO	Clamp Low Output Level	TA = 25℃, RL = 10kΩ to VCC	0.15	-	0.45	V
VCLP_HI	Clamp High Output Level	TA = 25℃, RL = 10kΩ to GND	4.55	-	4.85	V
TCLP	Clamp Low Output Level	TA=25°C, magnetic field step from：800 to 1200Gs, CL=1nF, SNST=2 mV/Gs	-	8	-	us
IND	Noise Density	Input-referenced noise density; TA = 25°C, SNST=6.88mV/Gs	-	1	-	mG/√Hz
PSRR_VOQ	Power Supply Rejection Ratio VOQ	DC~1kHz, 200mV pk-pk ripple on VCC, IP=0A	-	-40	-	dB
PSRR_VREF	Power Supply Rejection Ratio VREF	DC~1kHz, 200mV pk-pk ripple on VCC, IP=0A	-	-45	-	dB
PSRR_SNST	Power Supply Rejection Ratio SNST	DC~1kHz, 200mV pk-pk ripple on VCC, IP=IPR(max)	-	-35	-	dB
Accuracy Specification						
ELIN	Nonlinearity Sensitivity Error	TA = 25°C, VCC=5V	-0.5	±0.2	0.5	%
VREF	Reference Voltage	TA = 25°C, VCC=5V	2.49	2.5	2.51	V
VOE	Offset Error Voltage (VOQ-VREF)	TA = 25°C, VCC=5V	-10	-	10	mV
SNST_INIT	Initial Unprogrammed Sensitivity	TA = 25°C, VCC=5V	0.98	1	1.02	mV/Gs
			0.96	2	2.04	mV/Gs
			3.92	4	4.08	mV/Gs
			7.84	8	8.16	mV/Gs
			15.68	16	16.32	mV/Gs
ΔSNST_PKG	Sensitivity Drift Due to Package Hysteresis	TA = 25°C, temperature cycling：from 25°C to 150°C and back to 25°C	-	±1.25	-	%
Programming Specification						
VOQ_STEP	Average Quiescent Voltage Output Programming Step Size	TA = 25°C, VCC=5V	-	±1.25	-	mV
EVOQ_STEP	Quiescent Voltage Output Programming Resolution	TA = 25°C, VCC=5V	-	±0.625	-	mV
SNST_PR	Sensitivity Programmed Range	TA = 25°C, VCC=5V	0.6	-	1.4	mV/Gs
			1.4	-	2.8	mV/Gs
			2.8	-	5.6	mV/Gs
			5.6	-	11.2	mV/Gs
			11.2	-	22.4	mV/Gs
SNST_STEP	Average Sensitivity Programming Step Size	TA = 25°C, VCC=5V	-	±0.3125	-	%
ESNST_STEP	Sensitivity Programming Resolution	TA = 25°C, VCC=5V	-	±0.1562	-	%

Continued on the next page ...

Electrical Specifications(continued)

T_A=-40~150 ℃, V_{CC}=5V, C_{BYPASS}=0.1uF (unless otherwise specified)

Symbol	Parameters	Test Condition	Min	Typ	Max	Unit
Factory Temperature Coefficient Programed Specification						
ΔSNST_TC	Sensitivity Drift Through Temperature Range	TA = 25°C to 150°C	-2.0	-	2.0	%
		TA = –40°C to 25°C	-2.5	-	2.5	%
SNST_TC_STEP	Average Sensitivity Temperature Compensation Step Size		-	±0.07	-	%/℃
ΔVOE_TC	Offset Error Voltage Drift Through Temperature Range (VOQ-VREF)	TA = 25°C to 150°C	-15	-	15	mV
		TA = –40°C to 25°C	-15	-	15	mV
ΔVREF_TC	Reference Voltage Drift Through Temperature Range	TA = 25°C to 150°C	-15	-	15	mV
		TA = –40°C to 25°C	-15	-	15	mV
VOQ_TC_STEP	Average Quiescent Voltage Output Temperature Compensation Step Size		-	1.25	-	mV/℃
Lock Bit Programming						
EELOCK_BIT	EEPROM Lock Bit		-	1	-	bit

10 Characteristic Definitions

Power On Time---TPO

When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field.

The Power-On Time (TPO) is defined as the time taken between the supply reaching the minimum operating voltage VCCmin (t1), and the output voltage to settling to within ±10% of its steady state value under an applied magnetic field (t2) (See Figure 5).

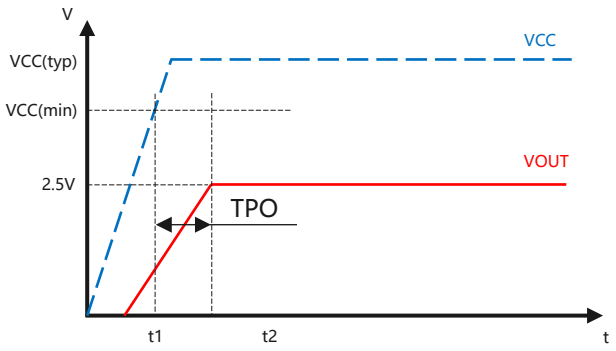


Figure.5 **Power On Time Definition**

Propagation Delay---TPD

The time interval between a) when the primary current signal reaches 20% of its final value, and b) when the output reaches 20% of its final value (see Figure 6).

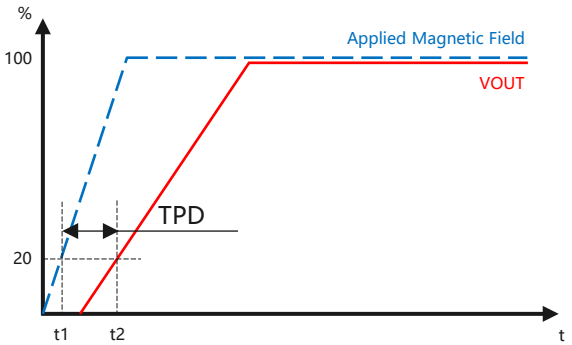


Figure.6 **Propagation Delay Definition**

Rise Time---TR

Rise Time is the time interval between the sensor VOUT reaching 10% of its full scale value (t1), and it reaching 90% of its full scale value (t2). (see Figure 7). Both TR and TRESP can be negatively affected by any eddy current losses created if a conductive ground plane is used.

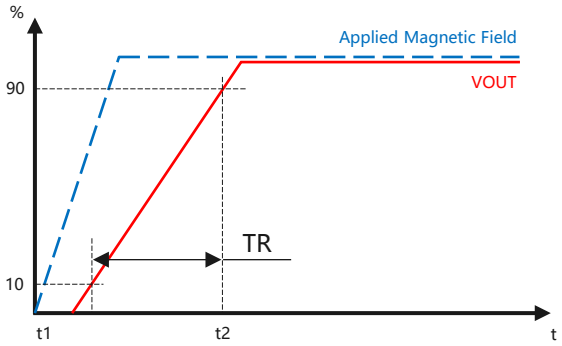


Figure.7 **Rise Time Definition**

Response Time---TRESP

The time interval between a) when the primary current signal reaches 80% of its final value, and b) when the sensor reaches 80% of its output corresponding to the applied current. (see Figure 8). Both TR and TRESP can be negatively affected by any eddy current losses created if a conductive ground plane is used.

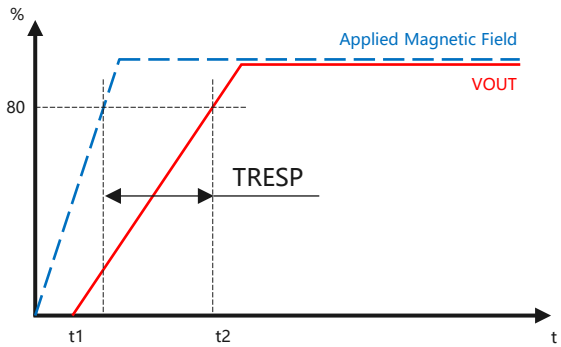


Figure.8 **Response Time Definition**

Delay to Clamp---TCLP

A large magnetic input step may cause the clamp to overshoot its steady state value. The Delay to Clamp (TCLP) is defined as the time it takes for the output voltage to settle within ±1% of its steady state value, after initially passing through its steady state voltage (see Figure 9).

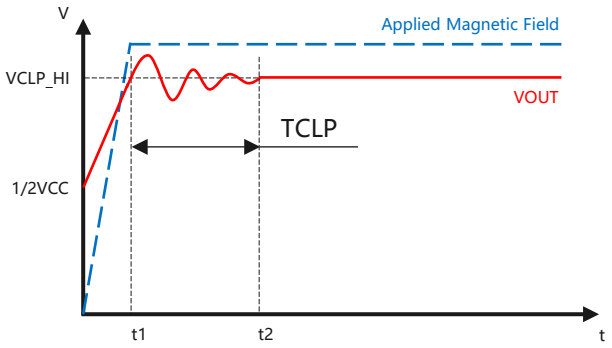


Figure.9 **Propagation Delay Definition**

Reference Voltage---VREF

The MT9512 provides a constant value output signal independent of the power supply. When VCC=4.5~5.5V, VREF=2.5V. This parameter has been calibrated at the factory. Customers can measure using the output pin alone or differential using the output pin and reference pin

Offset Error Voltage---VOE

Offset Error Voltage is the error voltage between the actual value of VOUT-VREF and the theoretical value (VOUT-VREF=0).
VOUT and VREF do not change with the change of power supply. When VCC = 4.5~5.5V (in the absence of magnetic field), VOUT = VREF = 2.5V.

Reference Voltage Through Temperature Range---ΔVREF_TC

Due to internal component errors and temperature influences, the Reference Voltage (VREF) may drift relative to typical values due to the influence of the operating ambient temperature (TA). Reference Voltage Through Temperature Range (ΔVREF_TC) is defined as:

$$\Delta VREF\_TC = VREF(TA) - VREF\_25℃$$

ΔVREF_TC should be calculated using actual measurements of VREF(TA) and VREF_25°C.

Sensitivity---SNST

The presence of a south polarity magnetic field, perpendicular to the branded surface of the package face, increases the output voltage from its quiescent value toward the supply voltage rail. The amount of the output voltage increase is proportional to the magnitude of the magnetic field applied.
Conversely, the application of a north polarity field decrease the output voltage from its quiescent value. This proportionality is specified as the magnetic sensitivity(Sens(mV/G)), of the device, and it is defined as:

$$SNST = \frac{V_{OUT(BPOS)} - V_{OUT(BNEG)}}{BPOS - BNEG}$$

where BPOS and BNEG are two magnetic fields with opposite polarities.

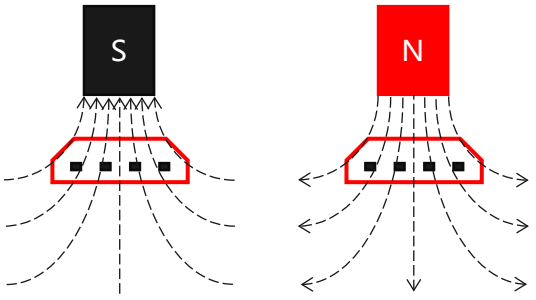


Figure.10 **Flux Direction Polarity**

Sensitivity Drift Through Temperature Range---ΔSNST_TC

Second order sensitivity temperance coefficient effects cause the magnetic sensitivity, to drift from its expected value over the operating ambient temperance range (TA). The Sensitivity Drift Through Temperature Range (Δ SNST_TC) is defined as:

$$\Delta SNST\_TC = \frac{SNST(TA) - SNST\_EXPECT(TA)}{SNST\_25℃} * 100\%$$

Power Supply Rejection Ratio VOQ ---PSRR_VOQ

It is defined as 20 x log of the ratio of the % change the VOQ over the % change in VCC reported as db in a specified frequency range.

$$PSRR\_VOQ=20\ lg\left|\frac{\Delta VOQ}{\Delta VCC}\right|$$

For Example:
When VCC changes from 5V to 4.5V (i.e. change -500mV), VOQ changes from 2.5V to 2.505V (i.e. change 5mV),then

$$PSRR\_VREF=20\ lg\left|\frac{5}{-500}\right|=-40dB$$

Power Supply Rejection Ratio VREF---PSRR_VREF

It is defined as 20 x log of the ratio of the % change the VREF over the % change in VCC reported as db in a specified frequency range.

$$PSRR\_VOQ=20\ lg\left|\frac{\Delta VREF}{\Delta VCC}\right|$$

For Example:
When VCC changes from 5V to 5.5V (i.e. change 500mV), the VREF changes from 2.5V to 2.497V (i.e. change -3mV),then

$$PSRR\_VREF=20\ lg\left|\frac{-3}{500}\right|=-44.437dB$$

Power Supply Rejection Ratio SNST---PSRR_SNST

It is defined as 20 x log of the ratio of the % change the SNST over the % change in VCC reported as db in a specified frequency range.

$$PSRR\_SNST=20\ lg\left|\frac{\Delta SNST\%}{\Delta VCC\%}\right|$$

For Example:
When VCC changes from 5V to 4.5V (i.e. change -500mV), the sensitivity changes from 8mV/GS to 7.992V (i.e. change -0.1%),then

则$PSRR_SNST=20\ lg\left|\frac{-0.1\%}{-10\%}\right|=-40dB$

Sensitivity Drift Due to Package Hysteresis---ΔSNST_PKG

Second order sensitivity temperature coefficient effects cause the magnetic sensitivity, to drift from its expected value over the operating ambient temperature range (TA). The Sensitivity Drift Through Temperature Range(Δ SNST_TC) is defined as:

$$\Delta SNST\_PKG=\frac{SNST\_25℃\_2-SNST\_25℃\_1}{SNST\_25℃\_1}*100\%$$

where SNST_25℃_1 is programmed value of sensitivity at TA=25℃, and SNST_25℃_2 is the value of sensitivity at TA=25℃, after temperature cycling from TA to 150℃/168 hours and back to 25℃

Nonlinearity Sensitivity Error---ELIN

Ideally input magnetic field vs sensor output function is a straight line. The non-linearity is an indication of the worst deviation from this straight line. The ELIN in % is defined as:

$$ELIN=\left(\frac{SNST\_B1}{SNST\_B2}-1\right)*100\%$$

Over Current Limit---ISCLP & ISCLN

The MT9512 has over-current protection function. When IOUT≥ISCLP or ISCLN, the output driver will be closed and the output will be turned into high resistance state.

Power-On Reset---POR, Undervoltage Lockout---UVL

The descriptions in this section assume temperature = 25°C, no output load (RL, CL) , and no significant magnetic field is present.

Power-Up. At power-up, as VCC ramps up, the output is in the following power supply voltage state. When VCC exceeds VPORH, the chip will enters the handshake protocol state. When VCC exceeds VUVLH, the output will go to 1/2*VCC or 2.5V, at this time, the chip is in normal working state.

Power-Down. If VCC drops below VUVLL, the output will be in a high-impedance state. If VCC drops below VPORL, the output is in the following power supply voltage state (See Figure. 11).

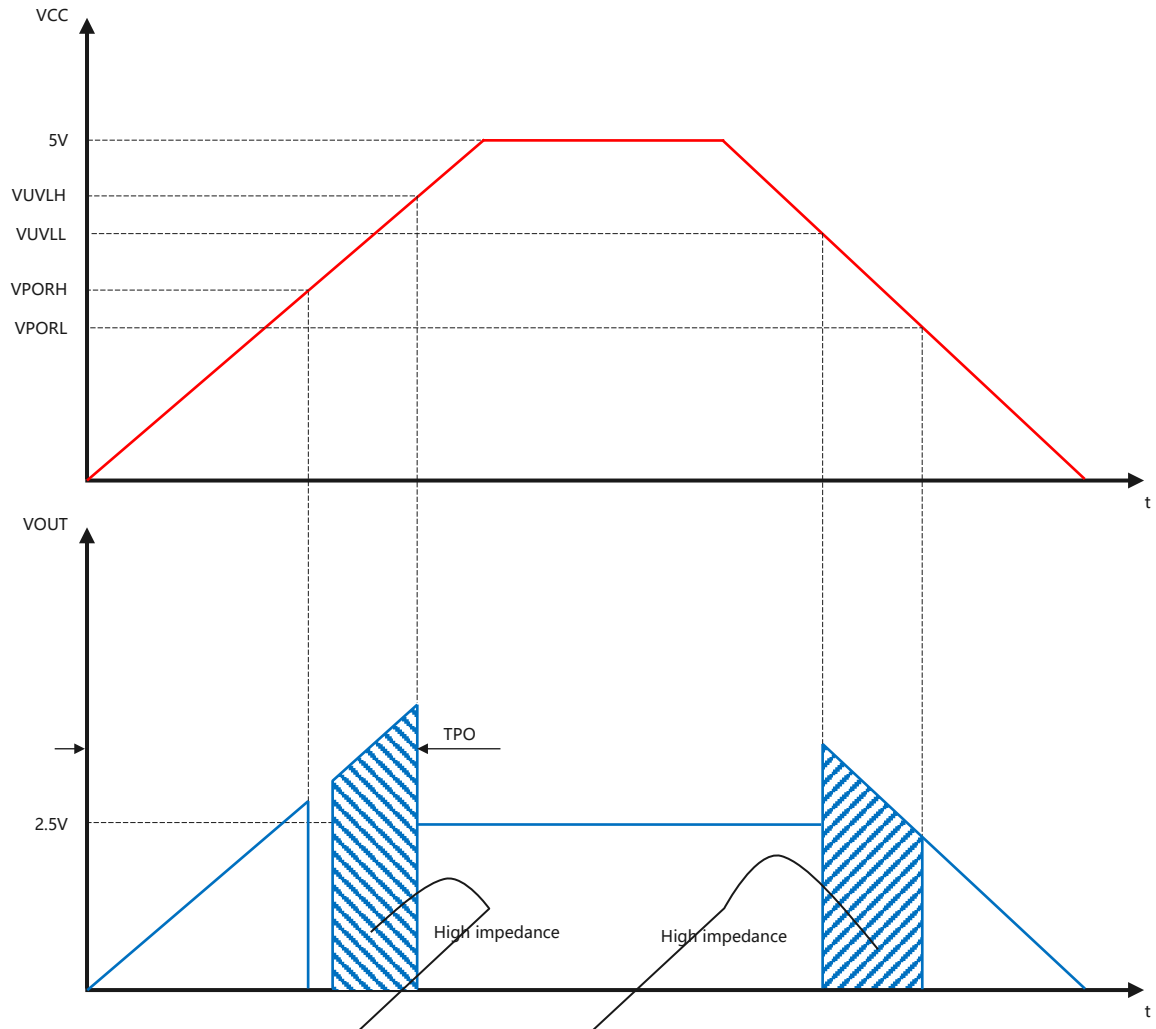
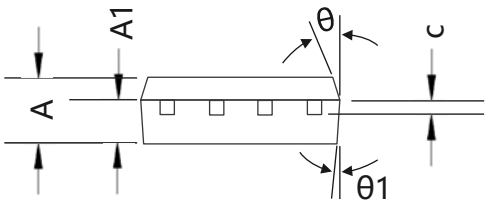
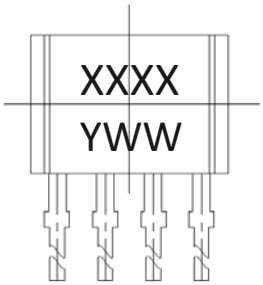


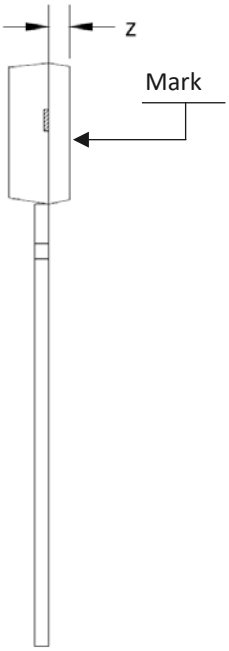
Figure.11 **POR and UVL Definition**

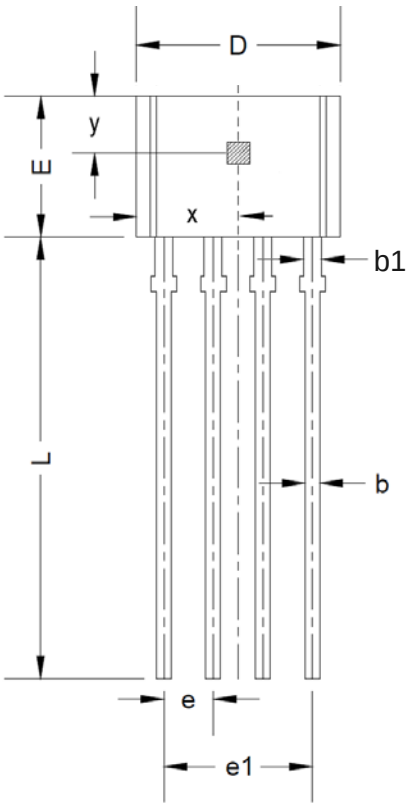
11 Package Material Information (For Reference Only – Not for Tooling Use)

11.1 SIP-4 Package Information









XXXX — Product ID

YWW — Data code (year week week)

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.460	1.660	0.057	0.065
A1	0.660	0.860	0.026	0.034
b	0.350	0.560	0.014	0.022
b1	0.380	0.550	0.015	0.022
c	0.360	0.510	0.014	0.020
D	5.120	5.320	0.202	0.209
E	3.550	3.750	0.140	0.148
e	1.270(BSC)		0.050(BSC)	
e1	3.810(BSC)		0.150(BSC)	
L	13.500	15.500	0.531	0.610
x	2.565(BSC)		0.101(BSC)	
y	0.772(BSC)		0.030(BSC)	
z	0.500(BSC)		0.020(BSC)	
Θ	11°		11°	
Θ1	6°		6°	

12 Copy Rights and Disclaimer

1. This document may not be reproduced or duplicated, in any form, in whole or in part without prior written consent of MagnTek .

2. MagnTek reserves the right to make changes to the information published in this document at anytime without notice.

3. MagnTek’ s products are limited for use in normal commercial applications. MagnTek’ s products are not to be used in any device or system, including but not limited to medical life support equipment and system.

For the latest version of this document, please visit our website: www.magntek.com.cn